Patent

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of:

Douglas — Examiner: Hassan, Aurangzeb

Application No.: 10/697,540 — **Art Group: 2182**

Filed: October 29, 2003

For: A Mechanism for Generating a Virtual Identifier

Mail Stop Appeal Brief – Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPEAL BRIEF
IN SUPPORT OF APPELLANT'S APPEAL
TO THE BOARD OF PATENT APPEALS AND INTERFERENCES

Sir:

Applicant (hereinafter "Appellant") hereby submits this Brief in support of its appeal from a final decision by the Examiner, mailed April 12, 2006, in the above-captioned case. Appellant respectfully requests consideration of this appeal by the Board of Patent Appeals and Interferences (hereinafter "Board") for allowance of the above-captioned patent application.

An oral hearing is not desired.

TABLE OF CONTENTS

I. REAL PARTY IN INTEREST

The invention is assigned to Intel Corporation, 2200 Mission College Boulevard, Santa Clara, California 95052, USA.

II. RELATED APPEALS AND INTERFERENCES

To the best of Appellant's knowledge, there are no appeals or interferences related to the present appeal that will directly affect, be directly affected by, or have a bearing on the Board's decision.

III. STATUS OF THE CLAIMS

Claims 1-29 are currently pending in the above-referenced application. No claims have been allowed. Claims 1-29 are the subject of this appeal.

IV. STATUS OF AMENDMENTS

In response to the Final Office Action, mailed on April 12, 2006, rejecting claims 1-29, Appellant filed a Response After Final under 37 C.F.R 1.116 on June 15, 2006. Appellant filed a Notice of Appeal on July 12, 2006. Subsequently, the Examiner mailed an Advisory Action on July 17, 2006 withdrawing a 35 U.S.C. §112 rejection, but maintaining various prior art rejections. In response,

A copy of all claims on appeal is attached hereto as an Appendix of Claims.

V. SUMMARY OF THE INVENTION

According to one embodiment, a method is disclosed. The method includes retrieving a first vendor identifier (ID) from a table, retrieving a second vendor ID from the table and-generating a virtual ID by randomizing the first vendor ID and the second vendor ID **(See operations 300-312 at Figure 3 and Specification at paragraphs [0031] – [0037])**.

According to another embodiment, an apparatus is disclosed. The computer apparatus includes a table to store two or more vendor identifiers (IDs) **(See table 46 at Figures 1 and 2 and Specification at paragraphs [0026] – [0028])**, circuitry to retrieve a first vendor ID and a second vendor ID from the table and to generate a virtual ID by randomizing the first vendor ID and the second vendor ID **(See circuitry 52 at Figure 1, and operations 302-312 at Figure 3)**.

Moreover, an article is disclosed having a storage medium having stored therein instructions) **(See Specification at paragraphs [0021] and [0022])**, that when executed by a machine result in retrieving a first vendor identifier (ID) from a table, retrieving a second vendor ID from the table and generating a virtual ID by randomizing the first vendor ID and the second vendor ID **(See operations 300-312 at Figure 3 and Specification at paragraphs [0031] – [0037])**.

In yet a further embodiment, a system is disclosed. The system includes a circuit board comprising a circuit card slot **(See motherboard 32 and circuit card slot 30 at Figure 1)** and a circuit card capable of being inserted into the slot **(See control circuit card 20 at Figure 1)**. The circuit card includes a table to store two or more vendor identifiers (IDs) **(See table 46 at Figures 1 and 2 and Specification at paragraphs**

[0026] – [0028]), and circuitry to retrieve a first vendor ID and a second vendor ID from the table and to generate a virtual ID by randomizing the first vendor ID and the second vendor ID **(See circuitry 52 at Figure 1, and operations 302-312 at Figure 3)**.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claims 1, 2, 5, 6, 7, 9, 10, 13, 14, 15, 17, 18, 21-23, 25-29 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Allen et al. (U.S. Patent No. 6,895,453) (hereinafter "*Allen*") in view of Ito et al. (U.S. Patent No. 6,684,209) (hereinafter "*Ito*") and further in view of Levitt (U.S. Patent No. 5,787,012) (hereinafter "*Levitt*").

Claims 3, 4, 8, 11, 12, 16, 19, 20 and 24 stand rejected under 35 U.S.C. §103(a) as being unpatentable over *Allen* in view of *Ito* and *Levitt* in further view of Hilton (U.S. Pub. No. 2004/0078401) (hereinafter "*Hilton*").

VII. ARGUMENTS

1. THE PENDING CLAIMS WERE IMPROPERLY REJECTED UNDER 35 U.S.C. § 103(a) BECAUSE THE COMBINATION OF *ALLEN, ITO* AND *LEVITT* DOES NOT DISCLOSE OR SUGGEST DOES NOT DISCLOSE OR SUGGEST EACH AND EVERY FEATURE OF THE PENDING CLAIMS

Appellant respectfully submits that *Allen* in view of *Ito* and *Levitt* fails to disclose or suggest the claimed invention for the reasons set forth below. As the Honorable Board is well aware, in order to establish a *prima facie* case of obviousness:

First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, *the prior art reference (or references when combined) must teach or suggest all the claim limitations*." (Emphasis added). *In re Vaech*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). Manual of Patent Examining Procedure (MPEP), 8th Edition, Revision 2, May 2004, §2143.

(A) Claims 1-4 and 7-19 were improperly rejected because *Allen* in view of *Ito* and *Levitt* does not disclose or suggest generating a virtual ID by randomizing a first vendor ID and a second vendor ID

Claims 1, 2, 5, 6, 7, 9, 10, 13, 14, 15, 17, 18, 21-23, 25-29 are not obvious in view of *Souissi* and *Watanabe* under 35 U.S.C. § 103(a). For example, Appellant's claim 1 recites:

> A method comprising:
> retrieving a first vendor identifier (ID) from a table;
> retrieving a second vendor ID from the table; and
> generating a virtual ID by randomizing the first vendor ID and the second vendor ID.

Appellant's claim 9 recites:

> An apparatus comprising:
> a table to store two or more vendor identifiers (IDs); and
> circuitry to retrieve a second vendor ID from the table; and
> circuitry to retrieve a first vendor ID and a second vendor ID from the table and to generate a virtual ID by randomizing the first vendor ID and the second vendor ID.

Appellant's claim 17 recites:

> An article comprising: a storage medium having stored therein instructions that when executed by a machine result in the following:
> retrieving a first vendor identifier (ID) from a table;
> retrieving a second vendor ID from the table; and
> generating a virtual ID by randomizing the first vendor ID and the second vendor ID.

Appellant's claim 25 recites:

> A system comprising:
> a circuit board comprising a circuit card slot; and
> a circuit card capable of being inserted into the slot, the circuit card comprising:
> a table to store two or more vendor identifiers (IDs); and
> circuitry to retrieve a first vendor ID and a second vendor ID from the table and to generate a virtual ID by randomizing the first vendor ID and the second vendor ID.

Allen discloses remote devices connected to a Fibre Channel network using a bridge. The bridge serves as a gateway to SCSI devices. Each of the SCSI devices includes a unique identifier. The respective device identifiers may include the vendor identifier for the device, the product identifier for the device, and the serial number corresponding to the device. *Allen* further discloses that the SCSI devices receive the

device identifier after a device swap occurs. This device identifier is compared with the previous device identifier. Because the device identifiers do not match, the Fibre Channel device determines that a SCSI device change has taken place and is able to take corrective action without compromising data integrity on either the SCSI device or in the Fibre Channel device attached to Fibre Channel interconnect. See *Allen* at col. 8, ll. 65 – col. 9, ll. 28.

Ito discloses a storage subsystem that can comprise a management table that defines relationships among information WWN which uniquely identifies an accessing host computer, a Logical Unit Number (LUN) in the storage subsystem which the host computer is permitted to access, and a Virtual Logical Unit Number (Virtual LUN) which is created from the LUN identifiers in any way of numbering in accordance with user's convenience. See *Ito* at col. 2, ll. 16-23.

Levitt discloses an integrated circuit that includes a first metal layer with first layer identification signal writing circuitry connections to produce first metal layer circuit identification signals. The integrated circuit also has a second metal layer with second layer identification signal writing circuitry connections to produce second metal layer circuit identification signals. Logic circuitry in the first metal layer has input connections to the first layer identification signal writing circuitry connections and the second layer identification signal writing circuitry connections. The logic circuitry combines the first metal layer circuit identification signals and the second metal layer circuit identification signals to produce a circuit identification number. The value of the circuit identification number can be changed by altering the first layer identification signal writing circuitry connectors or the second layer identification signal writing circuitry connections. Thus,

the value of the circuit identification number can be easily changed at the metal layer at which revisions are made. See *Levitt* at Abstract.

Appellant submits that any combination of *Allen*, *Ito* and *Levitt* fails to disclose or suggest generating a virtual ID by randomizing a first vendor ID and a second vendor ID. In fact, the Examiner admits that the combination of *Allen* and *Ito* fails to disclose or suggest generating a virtual ID by randomizing a first vendor ID and a second vendor ID. See Final Office Action at page 3, ll. 19 and 20. However, the Examiner relies on *Levitt* at (col. 5, ll. 42 - col. 6, ll. 5) to disclose a feature of generating a virtual ID by randomizing a first vendor ID and a second vendor ID. Id.

Col. 5, ll. 42 - col. 6, ll. 5 of *Levitt* recites:

> Returning now to FIG. 4, it can be seen that each connector 64A-64I is tied to a ground line. As a result, all inputs to the identification signal writing logic circuitry 40 are low. Consequently, the three bit circuit identification number stored in the identification register 32 is zero, a digital value of 000. Suppose now that a revision is made on the first metal layer M1 of the integrated circuit 35. This revision must be reflected in the value of the circuit identification number. That is, the value of the circuit identification number should now be 1, a digital value of 001. To accomplish this in accordance with the invention, the connector 64G is moved from its original position between the layer one ground line (Layer_1_ G) of block 62C to the layer one power line (Layer_ 1_ P) of block 62C. This change in the first layer identification signal writing circuitry connections 42 is shown in FIG. 6. (Note that the first layer identification signal writing circuitry connections 42 include the Layer._ 1_ P, Layer_ 1.sub_T, Layer_ 1_ G values in the three blocks 62A, 62B, and 62C).
>
> The change in electrical connections shown in FIG. 6 results in the required digital value of 001 stored in the identification register 32. Note that this change in value was accomplished simply by moving a connector of the first metal layer.

> Suppose now that modifications are required on the third metal layer M3. This necessitates a change in the circuit identification number from a value of 1 to 2, reflecting that two revisions have been made. The digital value for one is 001, while the digital value for two is 010. Note then that two bits in the identification register 32 must be changed to reflect the second version.

The above passage discloses logic circuitry that combines first metal layer circuit identification signals and a second metal layer circuit identification signals to produce a circuit identification number. Appellant submits that there is no disclosure in the passage of vendor IDs or virtual IDs in *Levitt*. Moreover, although there is a disclosure of combining metal layer circuit identification signals, combining is not equivalent to randomizing. Therefore, Appellant submits that **in no way can** *combining first and second metal layer circuit identification signals to produce a circuit identification number* **be considered equivalent to** *generating a virtual ID by randomizing a first vendor ID and a second vendor ID*.

Since *Allen*, *Ito* and *Levitt* all fail to disclose or suggest generating a virtual ID by randomizing a first vendor ID and a second vendor ID any combination of *Allen*, *Ito* and *Levitt* would also fail to disclose or suggest generating a virtual ID by randomizing a first vendor ID and a second vendor ID.

Further, Appellant submits that there is no suggestion or motivation provided in any of the references themselves to combine the teachings of *Allen*, *Ito* and *Levitt*. For instance, there would be no motivation for one of ordinary skill in the art to combine the integrated circuit with identification signal writing circuitry on multiple metal layers disclosed in *Levitt* with the mechanism for improved handling of fiber channel remote devices in *Allen*, and the security method for a storage subsystem disclose in *Ito*.

Therefore, the combining of *Allen*, *Ito* and *Levitt* is not a proper combination under §103 because it would be impermissible hindsight to combine the references.

Consequently, the Examiner has not established a prima facie case of obviousness, and the Examiner's rejection of claims 1, 9, 17 and 25 under 35 U.S.C. §103(a) as being obvious over the combination of *Allen, Ito* and *Levitt* is improper.

Claims 2-8 depend from claim 1, claims 10-16 depend from claim 9, claims 18-24 depend from claim 17 and claims 26-29 depend from claim 25. Given that dependent claims necessarily include the limitations of the claims from which they depend; Appellant submits that the invention as claimed in claims 2-8, 10-16, 18-24 and 26-29 are similarly patentable over the combination of *Allen*, *Ito* and *Levitt*.

For the forgoing reasons, Appellant submits that the Examiner has failed to search and find a printed publication or patent that discloses the claimed invention as set forth in MPEP § 706.02(a).

Thus, the Examiner erred in rejecting claims 1, 2, 5, 6, 7, 9, 10, 13, 14, 15, 17, 18, 21-23, 25-29 under 35 U.S.C. § 103(a).

2. THE PENDING CLAIMS 3, 4, 8, 11, 12, 16, 19, 20 AND 24 WERE IMPROPERLY REJECTED UNDER 35 U.S.C. § 103(a) BECAUSE THE COMBINATION OF *ALLEN*, *ITO*, *LEVITT* AND *HILTON* DOES NOT DISCLOSE OR SUGGEST DOES NOT DISCLOSE OR SUGGEST EACH AND EVERY FEATURE OF THE PENDING CLAIMS

Appellant respectfully submits that the combination of *Allen*, *Ito*, *Levitt* and *Hilton* fails to disclose or suggest the claimed invention for the reasons set forth below.

(A) Claims 3, 4, 8, 11, 12, 16, 19, 20 and 24 were improperly rejected because *Allen*, *Ito* and *Levitt* in view of *Hilton* does not disclose or suggest a certifying a first software-defined radio for operation if a first ID matches a second ID

Claims 3, 4, 8, 11, 12, 16, 19, 20 and 24 are not obvious under 35 U.S.C. §103(a) in view of *Allen*, *Ito*, *Levitt* and *Hilton*. Claims 3, 4 and 8, 11, 12 and 16, and 19, 20 and 24 depend from independent claims 1, 9 and 17, respectively, and necessarily include each of the features. As discussed above, the combination of *Allen*, *Ito* or *Levitt* does not disclose or suggest each and every element of Appellant's independent claims 1, 9 and 17. For example, *Allen*, *Ito* and *Levitt* each fail to disclose or suggest generating a virtual ID by randomizing a first vendor ID and a second vendor ID.

Hilton nondeterministic rounding of fixed point values in a digital signal processor. A pseudo-random value is generated and a preselcted number of pseudo-random bits are added to the result to be rounded prior to truncation being applied. Pseudo-random numbers may be generated by means including two maximal-length pseudo-random sequence generators. See *Hilton* at Abstract.

However, *Hilton* does not disclose or suggest a process of generating a virtual ID by randomizing a first vendor ID and a second vendor ID. Since *Allen*, *Ito*, *Levitt* and

Hilton individually do not disclose or suggest generating a virtual ID by randomizing a first vendor ID and a second vendor ID, any combination of *Allen*, *Ito*, *Levitt* and *Hilton* also would not disclose or suggest such a feature.

Moreover, Appellant submits that there is no motivation provided in any of the references themselves to combine *Allen*, *Ito*, *Levitt* and *Hilton*. Particularly, it would be impermissible hindsight based on Appellant's own disclosure to incorporate to combine the integrated circuit with identification signal writing circuitry on multiple metal layers disclosed in *Levitt* with the mechanism for improved handling of fiber channel remote devices in *Allen*, the security method for a storage subsystem disclose in *Ito* and *Hilton's* nondeterministic rounding of fixed point values in a digital signal processor. As a result, the combining of *Allen*, *Ito*, *Levitt* and *Hilton* is not a proper combination under §103.

Since the combination of *Allen*, *Ito*, *Levitt* and *Hilton* fails to disclose all of the elements required by Appellant's independent claim 1, the combination of *Allen*, *Ito*, *Levitt* and *Hilton* fails to teach or suggest each and every element of Appellant's invention as embodied in the claims. Consequently, the Examiner has not established a prima facie case of obviousness, and the Examiner's rejection of claims 3, 4, 8, 11, 12, 16, 19, 20 and 24 under 35 U.S.C. §103(a) as being obvious over *Allen*, *Ito* and *Levitt* in view of *Hilton* should be reversed.

VIII. CONCLUSION

Appellant respectfully submits that all the appealed claims in this application are patentable and request that the Board of Patent Appeals and Interferences overrule the Examiner and direct allowance of the rejected claims.

Appellant respectfully believes that the $500.00 to cover the appeal fee for one other than a small entity as specified in 37 C.F.R. § 1.17(c) is not necessary as it was paid on April 24, 2006 with the originally filed appeal brief. Please charge any shortages and credit any overpayment to out Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN

Date: September 12, 2006

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FIRST CLASS CERTIFICATE OF MAILING

I hereby certify that I am causing the above-referenced correspondence to be deposited with the United States Postal Service as first class mail with sufficient postage on the date indicated below and that this paper or fee has been addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450

Date of Deposit: September 12, 2006

Name of Person Mailing Correspondence: Leah Schwenke

Leah Schwenke 9/12/06

Signature Date

IX. APPENDIX OF CLAIMS (37 C.F.R. § 1.192(c)(9))

1. A method comprising:

retrieving a first vendor identifier (ID) from a table;

retrieving a second vendor ID from the table; and

generating a virtual ID by randomizing the first vendor ID and the second vendor ID.

2. The method of claim 1, wherein the process of generating the virtual ID comprises:

rotating the first vendor ID and the second vendor ID by a predetermined amount to form a rotated ID; and

performing a logical exclusive-or of the rotated ID with a predetermined number.

3. The method of claim 2, further comprising:

retrieving a value from a counter;

rotating the counter value to form a rotated counter value; and

performing a logical exclusive-or of the rotated counter value with the virtual ID.

4. The method of claim 3, wherein the counter value is based-upon an activation time.

5. The method of claim 1, further comprising:

retrieving a third vendor ID from the table;

rotating the third vendor ID by a predetermined amount to form a second rotated ID;

performing a logical exclusive-or of the second rotated ID with the virtual ID.

6. The method of claim 1, further comprising:

extracting the first vendor ID from a world wide name identifying a first device; and

extracting the second vendor ID from a world wide name identifying a second device.

7. The method of claim 6, wherein: the first device and the second device comprise physical devices.

8. The method of claim 3, wherein the counter is incremented using a timer routine.

9. An apparatus comprising:

a table to store two or more vendor identifiers (IDs); and

circuitry to retrieve a second vendor ID from the table; and

circuitry to retrieve a first vendor ID and a second vendor ID from the table and to generate a virtual ID by randomizing the first vendor ID and the second vendor ID.

10. The apparatus of claim 9, wherein the circuitry further rotates the first vendor ID

and the second vendor ID by a predetermined amount to form a rotated ID and performs a logical exclusive-or of the rotated ID with a predetermined number.

11. The apparatus of claim 10, wherein: the circuitry further retrieves a value from a counter, rotates the counter value to form a rotated counter value and performs a logical exclusive-or of the rotated counter value with the virtual ID.

12. The apparatus of claim 11, wherein the counter value is based upon an activation time.

13. The apparatus of claim 9, wherein the circuitry further retrieves a third vendor ID from the table, rotates the third vendor ID by a predetermined amount to form a second rotated ID and performs a logical exclusive-or of the second rotated ID with the virtual ID.

14. The apparatus of claim 13, wherein: the circuitry is also capable of extracting the first vendor ID from a world wide name identifying a first device; and extracting the second vendor ID from a world wide name identifying a second device.

15. (Previously Presented) The apparatus of claim 14, wherein the first device and the second device comprise physical devices.

16. The apparatus of claim 11, wherein the counter is incremented using a timer routine.

17. An article comprising: a storage medium having stored therein instructions that when executed by a machine result in the following:

retrieving a first vendor identifier (ID) from a table;

retrieving a second vendor ID from the table; and

generating a virtual ID by randomizing the first vendor ID and the second vendor ID.

18. The article of claim 17, wherein the process of generating the virtual ID comprises:

rotating the first vendor ID and the second vendor ID by a predetermined amount to form a rotated ID; and

performing a logical exclusive-or of the rotated ID with a predetermined number.

19. The article of claim 18, further comprising:

retrieving a value from a counter;

rotating the counter value to form a rotated counter value; and

performing a logical exclusive-or of the rotated counter value with the virtual ID.

20. The article of claim 19, wherein the counter value is based upon an activation time.

21. The article of claim 17, wherein the instructions when executed also result in:

retrieving a third vendor ID from the table;

rotating the third vendor ID by a predetermined amount to form a second rotated ID;

performing a logical exclusive-or of the second rotated ID with the virtual ID.

22. The article of claim 17, wherein the instructions when executed also result in: extracting the first vendor ID from a world wide name identifying a first device; and

extracting the second vendor ID from a world wide name identifying a second device.

23. The article of claim 22, wherein: the first device and the second device comprise physical devices.

24. The article of claim 19, wherein the counter is incremented using a timer routine.

25. A system comprising:

a circuit board comprising a circuit card slot; and

a circuit card capable of being inserted into the slot, the circuit card comprising:

a table to store two or more vendor identifiers (IDs); and

circuitry to retrieve a first vendor ID and a second vendor ID from the table and to generate a virtual ID by randomizing the first vendor ID and the second vendor ID.

26. The system of claim 25, wherein: the circuit board also comprises a processor coupled to a bus; and the circuit card slot is also coupled to the bus.

27. The system of claim 25, wherein: the first vendor ID corresponds to a first redundant array of inexpensive disk (RAID) and the second vendor ID corresponds to a second RAID.

28. The system of claim 27, wherein: the circuit card is coupled to the first RAID and the second RAID.

29. The system of claim 25, wherein: the circuit card is coupled to the first RAID and the second RAID via a network.

X. EVIDENCE APPENDIX

None.

XI. RELATED PROCEEDINGS APPENDIX

None.

FEE TRANSMITTAL for FY 2005

Patent fees are subject to annual revision.

☐ Applicant claims small entity status. See 37 CFR 1.27.

TOTAL AMOUNT OF PAYMENT ($) 500.00

Complete if Known	
Application Number	10/697,540
Filing Date	October 29, 2003
First Named Inventor	Chet R. Douglas
Examiner Name	Hassan, Aurangzeb
Art Unit	2182
Attorney Docket No.	42P17156

METHOD OF PAYMENT *(check all that apply)*

☐ Check ☐ Credit card ☐ Money Order ☐ None ☐ Other (please identify): _____

☒ Deposit Account Deposit Account Number: 02-2666 Deposit Account Name: Blakely, Sokoloff, Taylor & Zafman LLP

For the above-identified deposit account, the Director is hereby authorized to: (check all that apply)

☒ Charge fee(s) indicated below ☐ Charge fee(s) indicated below, except for the filing fee

☒ Charge any additional fee(s) or underpayment of fee(s) under 37 CFR §§ 1.16, 1.17, 1.18 and 1.20. ☒ Credit any overpayments

FEE CALCULATION

1. EXTRA CLAIM FEES

			Extra Claims		Fee from below		Fee Paid
Total Claims	29	- 29** =	0	x	50.00	=	$0.00
Independent Claims	4	- 4** =	0	x	200.00	=	$0.00
Multiple Dependent						=	

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
1202	50	2202	25	Claims in excess of 20
1201	200	2201	100	Independent claims in excess of 3
1203	360	2203	180	Multiple Dependent claim, if not paid
1204	790	2204	395	**Reissue independent claims over original patent
1205	300	2205	150	**Reissue claims in excess of 20 and over original patent

SUBTOTAL (1) ($) 0.00

***or number previously paid, if greater, For Reissues, see below*

2. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1051	130	2051	65	Surcharge - late filing fee or oath	
1052	50	2052	25	Surcharge - late provisional filing fee or cover sheet.	
2053	130	2053	130	Non-English specification	
1251	120	2251	60	Extension for reply within first month	
1252	450	2252	225	Extension for reply within second month	
1253	1,020	2253	510	Extension for reply within third month	
1254	1,590	2254	795	Extension for reply within fourth month	
1255	2,160	2255	1,080	Extension for reply within fifth month	
1401	500	2401	250	Notice of Appeal	
1402	500	2402	250	Filing a brief in support of an appeal	500.00
1403	1,000	2403	500	Request for oral hearing	
1451	1,510	2451	1,510	Petition to institute a public use proceeding	
1460	130	2460	130	Petitions to the Commissioner	
1807	50	1807	50	Processing fee under 37 CFR 1.17(q)	
1806	180	1806	180	Submission of Information Disclosure Stmt	
1809	790	1809	395	Filing a submission after final rejection (37 CFR § 1.129(a))	
1810	790	2810	395	For each additional invention to be examined (37 CFR § 1.129(b))	
Other fee (specify)					
				SUBTOTAL (2)	($) 500.00

SUBMITTED BY

Complete (if applicable)

Name (Print/Type)	Mark L. Watson	Registration No. (Attorney/Agent)	46,322	Telephone	(303) 740-1980
Signature				Date	09/12/06

Based on PTO/SB/17 (12-04) as modified by Blakely, Sokoloff, Taylor & Zafman (wlr) 12/15/2004.
SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450